REMARKS/DISCUSSION OF ISSUES

Claims 1-11 are pending in the application.

Applicant thanks the Examiner for acknowledging that the drawings are now accepted.

Reexamination and reconsideration are respectfully requested in view of the Remarks below.

35 U.S.C. § 103

The Office Action rejects claims 1-11 under 35 U.S.C. § 103 over Pechanek et al. U.S. patent 6,101, 592 ("Pechanek '592") in view of Pechanek et al. U.S. patent 6,173, 389 ("Pechanek '389").

Applicant respectfully traverses those rejections for at least the following reasons.

Claim 1

M.P.E.P. § 2143.03 provides that:

> *"All Claim Limitations Must Be Taught or Suggested. To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art."*

Among other things, the processing apparatus of claim 1 includes at least a first and a second issue slot, the first issue slot being controlled by a first control word, and the second issue slot being controlled by a second control word, wherein the width of the first control word is different from the width of the second control word.

Applicant respectfully submits that no combination of Pechanek '592 and Pechanek '389 would produce a processing apparatus including such a combination of features.

The Office Action cites col. 14, lines 41-45 of Pechanek '592 as supposedly

disclosing the recited issue slots, shown in FIG. 1 as execution unit 131 comprising "STORE," "LOAD," "ALU," "MAU," and "DSU," and shown in more detail in FIG. 8 as elements 840, 842, 844, 846 and 848.

However, Pechanek '592 does not disclose that a first one of these slots 840, 842, 844, 846 and 848 is controlled a first control word is different from the width of a second control word controlling a second one of the slots 840, 842, 844, 846 and 848. Indeed, to the contrary, Pechanek '592 teaches in the cited text at col. 14, lines 41-45 that "*each composite VIM entry preferably consists of 32-bit instruction slots (one per execution unit)*" and later, at col. 15, lines 62-66:

> "*If the instruction is a compacted instruction, then it is first expanded to its corresponding 32-bit format by translating bits and substituting register bits as required. After the expansion, the instruction is decoded as a normal 32-bit instruction.*"

See also, e.g., claims 1, 6 etc.

So, Pechanek '592 does not have different control slots that are controlled by control words having different widths.

Applicant notes that the Office Action cites instruction set format 16B in FIG. 1B of Pechanek '592 as supposedly disclosing that the width of a first control word for controlling a first issue slot is different that the width of a second control word for controlling a second issue slot.

Applicant respectfully disagrees. Instruction set format 16B merely shows that one format for a VLIW word may include a field with a 15 bit compacted instruction format and a field with a 30 bit instruction format. However, Pechanek '592 clearly teaches that these 15-bit compacted instructions are translated to 32 bit instructions (see e.g., FIGs. 4A-C) before control words are extracted and applied to the issue slots 840, 842, 844, 846 and 848– which are all the same size (see e.g., col. 14, lines 41-45).

Pechanek '389 does not remedy this shortcoming of Pechanek '592.

Therefore, no possible combination of Pechanek '592 and Pechanek '389 could produce the processing apparatus of claim 1.

Also among other things, in the processing apparatus of claim 1 each issue slot comprises a plurality of functional units.

The Office Action fairly admits that Pechanek '592 does not disclose such a feature. Furthermore, the Office Action does not allege that Pechanek '389 discloses such a feature either. Instead, the Office Action states that:

> "*one of ordinary skill in the art would be motivated to use the concept of multiple execution units per slot so that successive VLIW instructions which each had a sub-instruction destined for the same non-pipelined, multi-cycle execution unit would not find would not find* (sic) *one or more of the successive VLIW instructions blocked from execution by having to await the completion of one multi-cycle FP instruction in the slot for the one non-pipelines, multi-cycle execution unit*."1

Applicant respectfully disagrees.

Here, the Office Action does not cite anything in the prior art in support of its conclusory statement regarding what one of ordinary skill in the art supposedly would be motivated to do.

In response to the arguments in the previous Office Action that no evidence at all was provided in support of its assertion as to what one of ordinary skill in the art would supposedly do, the FINAL Office Action now cites *KSR Int'l Co. v. Teleflex, Inc., No. 04-1350 (U.S. April 30, 2007)*.

However, KSR states, in part:

> "*As is clear from cases such as Adams, a patent composed of several*

1 Applicant notes that this is a different rationale for the proposed combination that that offered in the

elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art,"

and

"*[a] factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning. See Graham, 383 U.S., at 36 (warning against a temptation to read into the prior art the teachings of the invention in issue and instructing courts to guard against slipping into the use of hindsight (quoting Monroe Auto Equipment Co. v. Heckethorn Mfg. & Supply Co., 332 F. 2d 406, 412 (CA6 1964)))*."

Here, Applicant respectfully submits that the proposed rationale for modifying Pechanek '592 is based merely on hindsight reconstruction.

First, the Office Action does not establish that Pechanek '592 even includes any non-pipelined, multi-cycle execution units (see, e.g. col. 15, lines 46-50; col. 16, lines 9-11, etc.).

Second, the Office Action does not explain how or why successive VLIW instructions which each had a sub-instruction destined for a same non-pipelined, multi-cycle execution unit would ever occur with Pechanek '592's manifold array architecture with multiple parallel processing elements.

Third, Pechanek '592 apparently teaches away from incorporating a plurality of functional units in its issue slots (see, e.g. col. 12, lines 40-43 and col. 14, lines 43-46).

Furthermore, Applicant respectfully submits that the Office Action includes no evidence or finding as to what the level of skill in the art was at the time of the invention. Absent such evidence and finding, it is not even possible to say what one

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first Office Action.

of ordinary skill in the art would or would not do.

So, Applicant respectfully submits that there is no basis for the proposed modification of Pechanek '592 to include a feature wherein each issue slot comprises a plurality of functional units.

Therefore, as the prior art does not include all of the features of Applicant's claim 1, Applicant's claim 1 is patentable under 35 U.S.C. § 103.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 1 is patentable over the cited prior art.

Claims 2-7

Claims 2-7 depend from claim 1 and are deemed patentable over the prior art for at least the reasons set forth above with respect to claim 1, and for the following additional reasons.

Claim 3

Among other things, in the processing apparatus of claim 3 the VLIW instruction is ***a compressed VLIW instruction, comprising dedicated bits for encoding of NOP operations***. Applicant respectfully submits that the cited prior art fails to disclose or suggest such a combination of features, and in particular Pechanek '592 does not disclose or suggest such features in the cited text at col. 16, lines 21-25. In that regard, FIG. 3B clearly shows that the NOPs are included as regular compacted 15-bit instructions within a VLIW, and are not encoded by dedicated bits within a VLIW.

Accordingly, for at least these additional reasons, Applicant respectfully submits that claim 3 is patentable over the cited art.

Claim 4

Among other things, the processing apparatus of claim 4 includes a decompression means for decompressing the compressed VLIW instruction and wherein the decompression means is conceived to derive information on the control word width using the dedicated bits. Applicant respectfully submits that the cited prior art fails to disclose or suggest such a combination of features, and in particular

Pechanek '592 does not disclose or suggest such features in the cited text at cols. 4, 5 and 6.

The Examiner now states that he considers the decompression means to be inherent in Pechanek '592.

Applicant disagrees, because: (1) Pechanek '592 does not disclose any compressed VLIWs, but instead only VLIWs which include within them compacted instructions; and (2) Pechanek '592 certainly does not disclose any dedicated bits for encoding of NOP operations, and therefore could not "inherently" include means that derives information on the control word width using such dedicated bits.

Accordingly, for at least these additional reasons, Applicant respectfully submits that claim 4 is patentable over the cited art.

Claim 8

Among other things, the method of claim 8 includes a first issue slot being controlled by a first control word, and a second issue slot being controlled by a second control word, wherein the width of the first control word is different from the width of the second control word.

For similar reasons to those set forth above with respect to claim 1, Applicant respectfully submits that the cited prior art, taken alone or collectively, does not suggest any method of processing data wherein a first issue slot is controlled by a first control word, and a second issue slot is controlled by a second control word, wherein the width of the first control word is different from the width of the second control word

Also among other things, the method of claim 8 includes processing data retrieved from a register file based on control signals generated from a set of instructions being executed in parallel, the set of instructions comprising at least a first and a second instruction, a first issue slot being controlled by a first control word corresponding to the first instruction and a second issue slot being controlled by a second control word corresponding to the second instruction, wherein the first and the second issue slots each comprise a plurality of functional units.

For similar reasons to those set forth above with respect to claim 1, Applicant respectfully submits that the cited prior art, taken alone or collectively, does not suggest any method of processing data where first and second instructions are processed in first and second issue slots each comprising a plurality of functional units.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 8 is patentable over the cited prior art.

Claims 9-11

Claims 9-11 all depend from claim 8 and are deemed patentable over the prior art for at least the reasons set forth above with respect to claim 1, and for the following additional reasons. Claims 10-11 include features similar to those recited above with respect to claims 3-4 and, respectively, and are deemed patentable for at least similar reasons to those set forth above with respect to claims 3-4.

CONCLUSION

In view of the foregoing explanations, Applicant respectfully requests that the Examiner reconsider and reexamine the present application, allow claims 1-11 and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283.0720 to discuss these matters.

Respectfully submitted,

VOLENTINE & WHITT

By: _____
Kenneth D. Springer
Registration No. 39,843

VOLENTINE & WHITT
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283.0724
Facsimile No.: (571) 283.0740